CLAIMS

1. An inspecting circuit of a semiconductor device characterized by comprising:

a plurality of input terminal which is inputted with signals from a plurality of signal lines respectively; and

two output terminals at which an output of inspection can be obtained,

wherein a determination whether the semiconductor device is normally operated or not is performed by two signals obtained at the two output terminals.

2. The inspecting circuit of a semiconductor device according to claim 1, characterized by comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

3. The inspecting circuit of a semiconductor device according to claim 1, characterized by comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

4. The inspecting circuit of a semiconductor device according to claim 3, characterized in that an ExNOR is used for the comparator circuit.

5. An inspecting circuit of a semiconductor device characterized by comprising;

an inspecting circuit having a plurality of signal output lines,

wherein the inspecting circuit comprises a plurality of input terminals to which signals from a plurality of signal output lines are inputted, and an output terminal at which an output of an inspection is obtained; and

a determination whether the semiconductor device is normally operated or not is performed by comparing an output pattern obtained at the output terminal by a signal inputted to the plurality of input terminals and a reference pattern.

6. The inspecting circuit of a semiconductor device according to claim 5, characterized by comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

7. The inspecting circuit of a semiconductor device according to claim 5,

characterized by comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

8. The inspecting circuit of a semiconductor device according to claim 7, characterized in that an ExNOR is used for the comparator circuit.

9. An inspecting circuit of a semiconductor device characterized by comprising:

an inspecting circuit having a source driver which inputs a clock signal, a start pulse and a video signal and outputs a signal to a plurality of source signal lines in

accordance with the clock signal, the start pulse and the video signal,

wherein the inspecting circuit comprises a plurality of input terminals to which signals outputted to the plurality of source signals are inputted respectively, and an output terminal at which an output of an inspection is obtained; and

wherein a determination whether the semiconductor device is normally operated or not is performed by comparing an output pattern obtained by a signal inputted to the plurality of input terminals and a reference pattern.

10. The inspecting circuit of a semiconductor device according to claim 9, characterized by comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

11. The inspecting circuit of a semiconductor device according to claim 9,

characterized by comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

12. The inspecting circuit of a semiconductor device according to claim 11, characterized in that an ExNOR is used for the comparator circuit.

13. An inspecting circuit of a semiconductor device, characterized by comprising:

an inspecting circuit having a gate driver which inputs a clock signal and a start pulse and sequentially outputs a select pulse to a plurality of source signal lines in

accordance with the clock signal and the start pulse,

wherein the inspecting circuit comprises a plurality of latch circuits which sample a signal for inspection in accordance with the select pulse which is outputted sequentially to the plurality of gate lines; and

a plurality of input terminals to which output signals from the plurality of latch circuits are inputted, and an output terminal at which an output of an inspection is obtained; and

wherein a determination whether the semiconductor device is normally operated or not is performed by comparing an output pattern obtained at the output terminal by a signal inputted to the plurality of input terminals and a reference pattern.

14. The inspecting circuit of a semiconductor device according to claim 13, characterized by comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an

inspection is obtained.

15. The inspecting circuit of a semiconductor device according to claim 13, characterized by comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

16. The inspecting circuit of a semiconductor device according to claim 15, characterized in that an ExNOR is used for the comparator circuit.

17. An inspecting circuit of a semiconductor device characterized by

comprising a plurality of NANDs, a plurality of NORs, and a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal a NOR of i-th line (i is an integer number of two or more) in the plurality or NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

18. An inspecting circuit of a semiconductor device characterized by comprising a plurality of NANDs, a plurality of NORs, a plurality of inverters, and a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through the inverter;

wherein an output terminal a NOR of i-th line (i is an integer number of two or more) in the plurality or NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through the inverter;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of

NANDs is electrically connected to a first input terminal of the comparator circuit;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to a second input terminal of the comparator circuit; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

19. The inspecting circuit of a semiconductor device according to claim 18, characterized in that an ExNOR is used for the comparator circuit.

20. An inspecting method of a semiconductor device characterized by comprising the steps of:

inputting signals outputted to all of a plurality of output signal lines to an inspecting circuit simultaneously;

obtaining an output pattern from the inspecting circuit; and

determining an operation of the semiconductor device to be good or defective by comparing the output pattern and a reference pattern.

21. An inspecting method of a semiconductor device, characterized by comprising the steps of:

sampling signals for inspection sequentially in accordance with signals outputted sequentially from a plurality of output signal lines;

inputting all of the sampled signals for inspection to an inspecting circuit simultaneously;

obtaining an output pattern from the inspecting circuit; and

determining an operation of the semiconductor device to be good or defective by comparing the output pattern and a reference pattern.